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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,842	01/16/2004	Haining S. Yang	FIS920030238	1841

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EXAMINER	
LINDSAY JR, WALTER LEE	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 12/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/707,842	YANG ET AL.
	Examiner	Art Unit
	Walter L. Lindsay, Jr.	2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-17,19 and 25-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17* is/are allowed.

6)☒ Claim(s) *8-16,19 and 25-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an After final amendment filed on 11/28/05.

Currently, claims 8-17, 19 and 25-32 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 8-14 and 19, 25-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U.S. Patent No. 6,153,501 dated 11/28/2000) in view of Chen et al. (U.S. Publication No. 2005/0136583 filed 12/23/2003).

Becker shows the method substantially as claimed in Figs. 5 and 6 and corresponding text as: depositing a layer of nitride film (62A) over a gate stack (52A, will represent the stack) and a surface of a substrate (50) (col. 2, lines 44-62); removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack (col. 3, lines 8-16) (claims 8 and 19). Becker teaches that a resist

material (64) is deposited on a surface of the nitride film over the substrate while leaving a surface of the nitride film proximate an upper portion of the gate stack (col. 3, lines 8-16) (claims 9 and 25). Becker teaches the removal of an upper portion of the gate stack and the nitride film disposed thereon (col. 3, lines 17-25) (claims 10 and 26). Becker teaches that depositing the resist comprises depositing one of a spin-on material, an anti-reflection coating, an oxide film, and a low k material (col. 3, lines 8-16) (claims 11 and 27). Becker teaches that spacers are formed at a lower portion of the sidewalls of the gate stack (col. 3, lines 8-16) (claims 12 and 28). Becker teaches that the spacers are formed includes forming the spacers along substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls (col. 3, lines 8-16) (claims 13 and 29). Becker teaches that depositing a resist comprises depositing at least one of an oxide layer or a borophosphorsilicate glass on low spots and leaving high spots exposed (col. 3, lines 8-16) (claims 14 and 30).

Becker lacks anticipation only in not explicitly teaching that: 1) the gate is about 60nm wide, a spacer is about 50 nm wide, and the nitride film provides a stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately $4.5x10^9$ dynes/cm^2 at about 5 nm below a gate oxide (claim 8); and 2) the gate is about 60nm wide, a spacer is about 50 nm wide, and the nitride film provides a stress of about 2.0 GPa, the enhanced stress in the transistor channel is greater than approximately $5.5x10^9$ dynes/cm^2 at about 5 nm below a gate oxide (claim 19).

As it pertains to the gate width and spacer width and depth of channel:

Given the teaching of the references, it would have been obvious to determine the optimum thickness, temperature as well as condition of delivery of the layers involved. See In re Aller, Lacey and Hall (10 USPQ 233-237) It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 f.2d 1575,1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

Chen forms an advanced strained-channel technique to improve CMOS performance. A silicon nitride layer (24) is formed with a tensile stress preferably from about $1x10^9$ to $2x10^{10}$ dyne/cm^2 [0035-0038]. The from about 1 to 2 GPa high tensile stress film can largely enhance the channel strain and this tensile stress is tunable by temperature or the gas ratio for specific applications [0049]. The capping layer exhibits good thickness uniformity, step coverage and pattern loading effect and may serve as a resist protect layer without additional oxide RPO formation and reduces STI loss [0069].

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify Becker, by having a stress layer formed at levels greater than 4.5x109 dynes/cm2, as taught by Chen, with the motivation that Chen teaches a capping layer exhibits good thickness uniformity, step coverage and pattern loading effect and may serve as a resist protect layer without additional oxide RPO formation and reduces STI loss.

1. Claims 15-16 and 31-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U.S. Patent No. 6,153,501 dated 11/28/2000) in view of Chen et al. (U.S. Publication No. 2005/0136583 filed 12/23/2003) and Pan et al. (U.S. Patent No. 6,198,144 dated 3/6/2001).

Becker as modified by Chen shows the method substantially as claimed in the preceding paragraph.

Becker as modified by Chen lacks anticipation only in not explicitly teaching that: 1) removing a portion of the gate stack and the nitride film disposed thereon comprises reactive ion etching (claim 15); and 2) removing a portion of the gate stack and the nitride film disposed thereon comprises chemical mechanical polishing (claim 16).

Pan shows the formation of spacers that only cover lower portions of the gate stack and that a nitride film is deposited by (PECVD). Layer 22 is then formed over the substrate and gate stack, this layer is formed by PECVD, it can then be reduced and etch by reactive ion etching techniques (col. 5, lines 33-51). The advantages of these techniques aids in providing thicker portions on the horizontal portions (substrate) and thinner on vertical surfaces (gate stack) (col. 2, lines 54-64). Another advantage is the fact that the nitride film reduces the conversion of conductive layers into non – conductive layers (col. 3, lines 16-32). Chemical mechanical polishing is well known and often used in etching nitride films.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Becker by etching a nitride film by reactive ion etching and chemical mechanical polishing, as taught by Pan with the motivation

that Pan teaches that thicker portions of deposited layers are formed on horizontal portions while thinner portions are formed on vertical portions and the nitride film reduces the conversion of conductive layers into non-conductive layers.

Response to Arguments

2. Applicant's arguments filed on 7/21/2005 in Application No. 10/707,842 have been fully considered but they are not persuasive. The examiner views the teaching of Doshi towards forming a good barrier with minimum thickness that lays in the range of 65 - 250Å teaches that the thicker portions of the nitride layer would be formed over the portions that need the most protection and thinner over those portions such as the gate stack which do not. The examiner views Becker as performing the same operation of removing a nitride layer, as the claimed invention.

Allowable Subject Matter

3. Claims 17 is allowed.

4. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...forming a spacer adjacent a sidewall of the gate stack; and

etching upper portions of the spacer to form sidewalls only at lower portions of the gate stack, as required by claim 17.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
December 21, 2005